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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,406	07/24/2003	Andre DeHon	B-5174NP 621116-2	2819

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,406	DEHON ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- Th MAILING DATE of this communication appears on th cover sheet with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19-22,26-35 and 37-47* is/are rejected.

7)☒ Claim(s) *18,23-25 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 07/24/2003 is acceptable.

Claim Rejections

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-17, 19-22, 26-35, and 37-47** are rejected under 35 U.S.C. 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kuekes et al. U.S. Patent 6,256,767 (the '767 patent, which is cited by Applicant).

The '767 patent discloses in the figures and respective portions of the specification, particularly the claims, a memory array, a logic arrangement, and an inherent method of fabricating thereof, as claimed. In particular, although Figure 6 depicts a structure with only one

demultiplexer, claim 16 calls for a second demultiplexer. Similarly, although the figures depict molecular wires 12 and 14 as nanoscale wires, claim 11 refers to these wires as either nanoscale wires or microscale wires ("both of said two wires have a thickness that ranges from sub-micrometer to micrometer").

Referring to **claim 1**, the '767 patent discloses a memory array comprising:

a first set of nanoscale wires 14 (Fig. 6);

a second set of nanoscale wires 12 intersecting the first set of nanoscale wires, intersections between the first set and the second set defining memory locations (column 3, lines 30+, "...to communicate with the nanoscopic arrays of wires which make up logic, memory, and interconnect of the molecular wire system, and of transferring data into and out of a system with an enormous number of elements by using an input/output circuit with a much smaller number of elements");

wherein the memory locations are addressed by selecting one nanoscale wire of the first set of nanoscale wires 14 and one wire of the second set of nanoscale wires 12 (claim 16, and note that a second demultiplexer, as claimed by claim 16, would comprise a second set of address lines 34, which would select one wire of the second set of nanoscale wires 12. This same remark shall be applied to other components inherent in the second demultiplexer as rightfully claimed by the '767 patent in claims 1 and 16; and hereinafter will be simply refereed to as *"claim 16"*);

wherein nanoscale wires of the first set and nanoscale wires of the second set comprise controllable regions, generally defined as 36 in Fig. 6 or 36' or 38 or 40 in Fig. 8, in conjunction with *"claim 16"*, axially distributed along the nanoscale wires, a first set of the controllable

regions exhibiting a first physical property, and a second set of the controllable regions exhibiting a second physical property, different from the first physical property;

the memory array further comprising:

a first plurality of addressing wires 34, each addressing wire of the first plurality associated with a series of regions of the first set of nanoscale wires 14; and

a second plurality of addressing wires (*"claim 16"*), each addressing wire of the second plurality associated with a series of regions of the second set of nanoscale wires 12

Referring to **claim 21**, the '767 patent discloses a circuit for selecting a nanoscale wire among a plurality of nanoscale wires, comprising:

microscale ohmic contacts 38 or 40, Fig. 8 or Fig. 10, in conjunction with *"claim 16"*, each ohmic contact connected to a different subset of the plurality of nanoscale wires for selecting a specific subset of the plurality of nanoscale wires; and

addressing wires 34 associated with the different subsets of the plurality of nanoscale wires 14 and 12, for selecting a nanoscale wire among the specific subset of nanoscale wires once the specific subset has been selected, column 9, lines 36+:

> "As shown in FIG. 8, all of the molecular wires 14 are shorted together by a conductor 38 at one end so as to be driven by a single conventional CMOS driver 40. But in the array 30 itself at the right, only one of the molecular wires is effectively biased. Exactly one wire has a low resistance path to the driver 40. The particular wire that is addressed is the only one to have all of the transistors in series in the conducting low resistance state. The other (N-1) wires have high resistance paths."

Regarding **claim 26**, the '767 patent discloses a memory array comprising:

a plurality of nanoscale wires 14 (Figure 6);

a first set of microscale wires 34 ("address lines") intersecting the nanoscale wires 14, intersections between the first set of microscale wires address lines and the nanoscale wires defining address locations to address one or more nanoscale wires among the plurality of nanoscale wires; and

a second set of microscale (claim 11, "both of said two wires have a thickness that ranges from sub-micrometer to micrometer") wires 12 intersecting the nanoscale wires 14, intersections between the second set of microscale wires and the nanoscale wires defining memory locations (column 3, lines 30+, "...to communicate with the nanoscopic arrays of wires which make up logic, memory, and interconnect of the molecular wire system, and of transferring data into and out of a system with an enormous number of elements by using an input/output circuit with a much smaller number of elements").

Referring to **claim 27**, the '767 patent further discloses that the memory locations are selected by selecting one nanoscale wire 14 and one microscale wire of the second set of microscale wires 12.

Referring to **claim 28**, the '767 patent further discloses that the nanoscale wires 14 comprise controllable regions, generally defined as 36 in Fig. 6 or 36' or 38 or 40 in Fig. 8, in conjunction with *"claim 16"*, axially distributed along the nanoscale wires, a first set of the controllable regions exhibiting a first physical property, and a second set of the controllable regions exhibiting a second physical property, different from the first physical property.

Referring to **claim 37**, the '767 patent discloses a three-dimensional memory array comprising: a plurality of layers of nanoscale wires 12 and 14, intersections between nanoscale wires of a first layer and nanoscale wires of a second layer adjacent to the first layer defining memory locations;

a plurality of microscale contacts 38 or 40, Fig. 8 or Fig. 10, in conjunction with "claim 16", connected to nanoscale wires of different layers of nanoscale wires; wherein the nanoscale wires comprise controllable regions, generally defined as 36 in Fig. 6 or 36' or 38 or 40 in Fig. 8, in conjunction with *"claim 16"*, axially distributed along the nanoscale wires, to allow addressing of the nanoscale wires, a first set of the controllable regions exhibiting a first physical property, and a second set of the controllable regions exhibiting a second physical property, different from the first physical property.

Referring to **claim 41**, the '767 patent discloses a process for manufacturing a logic arrangement having microscale and nanoscale wires, comprising:

providing microscale wires 34 (Fig. 6) and 34, not shown in Fig. 6 but claimed in *"claim 16"*;

determining an addressing portion on the microscale wires 34 ("address lines");

transferring a first set of aligned nanoscale wires 14 over the microscale wires 34; and

transferring a second set of aligned nanoscale wires 12 over the microscale wires 34 (*"claim 16"*) and the first set of nanoscale wires 14, orthogonally to the first set of nanoscale wires.

Regarding **claims 2, 3, 31, and 32**, the '767 patent further discloses that the first set of controllable regions allow conduction along the nanoscale wire when each region of the first set

is either controlled with a signal having a value lower that a first threshold or is not controlled (column 7, last paragraph).

Referring to **claims 4 and 29**, the '767 patent further discloses that the difference between the first physical property and the second physical property is based on different doping levels of the controllable regions (column 8, last two paragraphs).

Referring to **claims 5, 16, and 30,** the figures of the '767 patent further depict that the difference between the first physical property and the second physical property of the controllable regions 36 in Fig. 6 or 36' or 38 or 40 in Fig. 8 is based on different materials.

Referring to **claims 6-9 and 33-34,** the '767 patent discloses a memory array as claimed and as detailed above including cells to be used as memory and to be addressed but fails to explicitly disclose that the memory cells are to be involved in reading and writing operations. Nevertheless, in column 4, under the Definitions Section, the patentee refers to PROM and RAM. More importantly, since the disclosure does not exclude these operations, it would appear that the '767 patent's memory array could function with reading and writing operations.

Referring to **claims 10-11, 19-20, 35, and 39,** the '767 patent further discloses microscale wires acting as microscale ohmic contacts, generally depicted as 38 or 40, Fig. 8 or Fig. 10, in conjunction with *"claim 16"*, each ohmic contact connected to a different subset of the plurality of nanoscale wires for selecting a specific subset of the plurality of nanoscale wires, and the microscale wires allowing signals to be disconnected from the nanoscale wires.

Referring to **claims 12-15,** the '767 patent further discloses microscale wires 38 or 40, Fig. 8 or Fig. 10, in conjunction with *"claim 16"*, or discloses that the addressing wires 34 are microscale wires, that the microscale wires 38 or 40 or 34 control FET-controllable regions,

generally defined as 36 (Fig. 6) or 36' (Fig. 8) or 10. The '767 patent further discloses that the memory locations are defined by means of programmable diode-type crossbar junctions between the first set and the second set (Fig. 3), that the memory locations are defined by means of FET-type crossbar junctions between the first set and the second set (column 8, lines 19+), and that nanoscale wires of one set among the first set and a second set of nanoscale wires comprise controllable doped regions radially distributed along the nanoscale wires, the radially distributed controllable doped regions allowing information to be stored at the memory locations (column 8, last paragraph).

Referring to **claims 17 and 22,** addressing wires 34 are microscale wires ("lithographic wires").

Referring to **claims 38 and 40,** the '767 patent discloses a multi-dimensional memory array as claimed including first layer of memory-location-defining nanoscale wires, a second layer of memory-location-defining nanoscale wires. However, the reference fails to disclose repeating occurrences of adjacent sets of the layers, and thus also fails to disclose a necessary layer of insulating nanoscale wires before repeating the occurrences of adjacent sets of the layers. Nevertheless, the change would have been obvious for at least one of the following two reasons: 1) it would have been obvious to one of ordinary skill in the art at the time the invention was made to repeat occurrences of adjacent sets of the layers (and thus would have to add a necessary layer of insulating nanoscale wires before repeating the occurrences of adjacent sets of the layers); and 2) one would have been motivated to repeat occurrences of adjacent sets of the layers simply to save precious space.

Referring to **claims 42-47,** the '767 discloses forming a nanoscale memory as claimed and as detailed above including forming nanoscale wires 12 and 14 by doping, but fails to disclose that the doping of the nanoscale wires 12 and 14 is by doping axially and/or radially as claimed. Nevertheless, the process would have been obvious for at least one of the following two reasons: 1) at the time the invention was made, the process was known (see, for example, U.S. Patent Application Publication 2003/0089899 by Lieber et al., paragraph [0507]); and 2) the process was one of a variety of processes one of ordinary skill in the art at the time the invention was made would perform for the purpose of providing nanoscale wires.

Allowable Subject Matter

3. **Claims 18, 23-25, and 36** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a nanoscale device comprising cross-point nanoscale wires and addressing lines, having all exclusive limitations as recited in claims 1/18 (claims 1 and 18), 21/23, 21/24, 21/25, and 21/36, characterized in that the addressing lines are also nanoscale wires or that microscale ohmic contacts, each of which is connected to a different subset of the nanoscale wires for selecting a specific subset of the nanoscale wires, are staggered or designed to leave not more than a sub-lithographic sized gap of unaddressed nanoscale wires between them.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Application Publication 2003/0206436 by Eaton, Jr. et al. discloses a molecular wire crossbar flash memory.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tu-Tu Ho
June 18, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800